REMARKS

Claims 1, 2 and 4 are pending in this application, of which claim 1 has been amended. Claim 3 has been canceled. No new claims have been added.

Claims 1-4 stand rejected under 35 U.S.C. § 103(a) as unpatentable over **Robinson et al.** in view of **Kawasaki et al.** (both previously applied), U.S. Patent 5,940,444 to Jenkin et al. (hereafter, "**Jenkin et al.**") and Kawahara, "20-Mb/s Erase/Record Flash Memory by Asymmetrical Operation", 1996 (hereafter, "**Kawahara**").

Applicants respectfully traverse this rejection.

Robinson et al. discloses a flash memory card with a power control register that is used to place certain flash memories in a power down mode.

Column 2, lines 6-12 disclose:

> One type of prior flash EPROM used in a prior flash memory card has a standby mode that disables most of the flash EPROM circuitry and reduces device power consumption. The prior flash EPROM also has an active mode. The active mode requires increased power consumption. The active mode is used when the flash EPROM is being written to, read from, or erased.

The Examiner has admitted that **Robinson et al.** does not disclose the buffer memory that data is read into and that when the amount of data stored in the memory falls below a threshold the memory card is then operated in the active mode, as recited in claim 1 of the instant application.

Kawasaki et al. discloses a disk control apparatus comprising a disk controller for controlling a circuit which controls read operation for reading data from a disk and a CPU for controlling the circuit and the disk controller. The disk controller comprises a buffer memory for storing data for being transferred between a host and the disk controller and a notification section for notifying the CPU that a first state in which an all buffer region of the buffer memory is stored with data to be transferred to the host transmits to a second state in which a predetermined space occurs in the buffer region of the buffer memory as a result of transferring data to the host. The CPU comprises a main control section for stopping power supply to the circuit during the first state and for supplying power to the circuit in response to a notification from the notification section.

Kawasaki et al. teaches only one powered state, which occurs only when a predetermined space occurs in the buffer region by transferring data to the host. The other state in which the buffer is completely full of data to be transferred to the host, consumes no power.

This is in contrast to the present invention, in which there are two power on states, where one is a high (active) mode for reading data from the memory card to the buffer at a high bit rate, and the other is a low (standby) mode in which the memory card waits for a next memory access while the buffer outputs data at a low rate.

Jenkin et al. and **Kawahara** have been cited for teaching the data rates of 128 Kbps and 8 Mbps, respectively.

The Examiner has cited column 2, line 50 to column 3, line 49 of **Robinson et al.** for teaching that the controller of the memory card can operate the card under two current consumption modes, an active and a standby mode.

Applicants respectfully disagree. This passage indicates that active, standby and power-off modes for the flash memory are selected upon receipt of first through sixth signals. This is in contrast to the present invention as recited in claim 3, which recites that "the controller...is so constructed that the standby mode follows when there is no memory access within a predetermined period of time after setting the active mode." Thus, the standby mode occurs automatically after the lapse of the predetermined period of time without the need for a control signal to trigger it. **Robinson et al.** teaches an active mode, a standby mode, and a power down mode, and the power down mode (power off), not the standby mode (low power consumption state), follows when there is no memory access within a predetermined period of time (column 16, lines 16-24). **Robinson et al.** fails to disclose the predetermined period of time recited in claim 3, and **Kawasaki et al.** discloses an on/off-controls power supply, and teaches only one powered state (on state). Thus, the combination of **Robinson et al.** and **Kawasaki et al.** fails to teach, mention or suggest the present invention, in which the standby mode (low power consumption state) follows when there is no memory access within a predetermined period of time.

Accordingly, claim 3 has been canceled and its limitations have been added to claim 1. Thus, the 35 U.S.C. § 103(a) rejection should be withdrawn.

In view of the aforementioned amendments and accompanying remarks, claims 1, 2 and 4, as amended, are in condition for allowance, which action, at an early date, is requested.

If, for any reason, it is felt that this application is not now in condition for allowance, the Examiner is requested to contact Applicants' undersigned attorney at the telephone number indicated below to arrange for an interview to expedite the disposition of this case.

In the event that this paper is not timely filed, Applicants respectfully petition for an appropriate extension of time. Please charge any fees for such an extension of time and any other fees which may be due with respect to this paper, to Deposit Account No. 01-2340.

Respectfully submitted,

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